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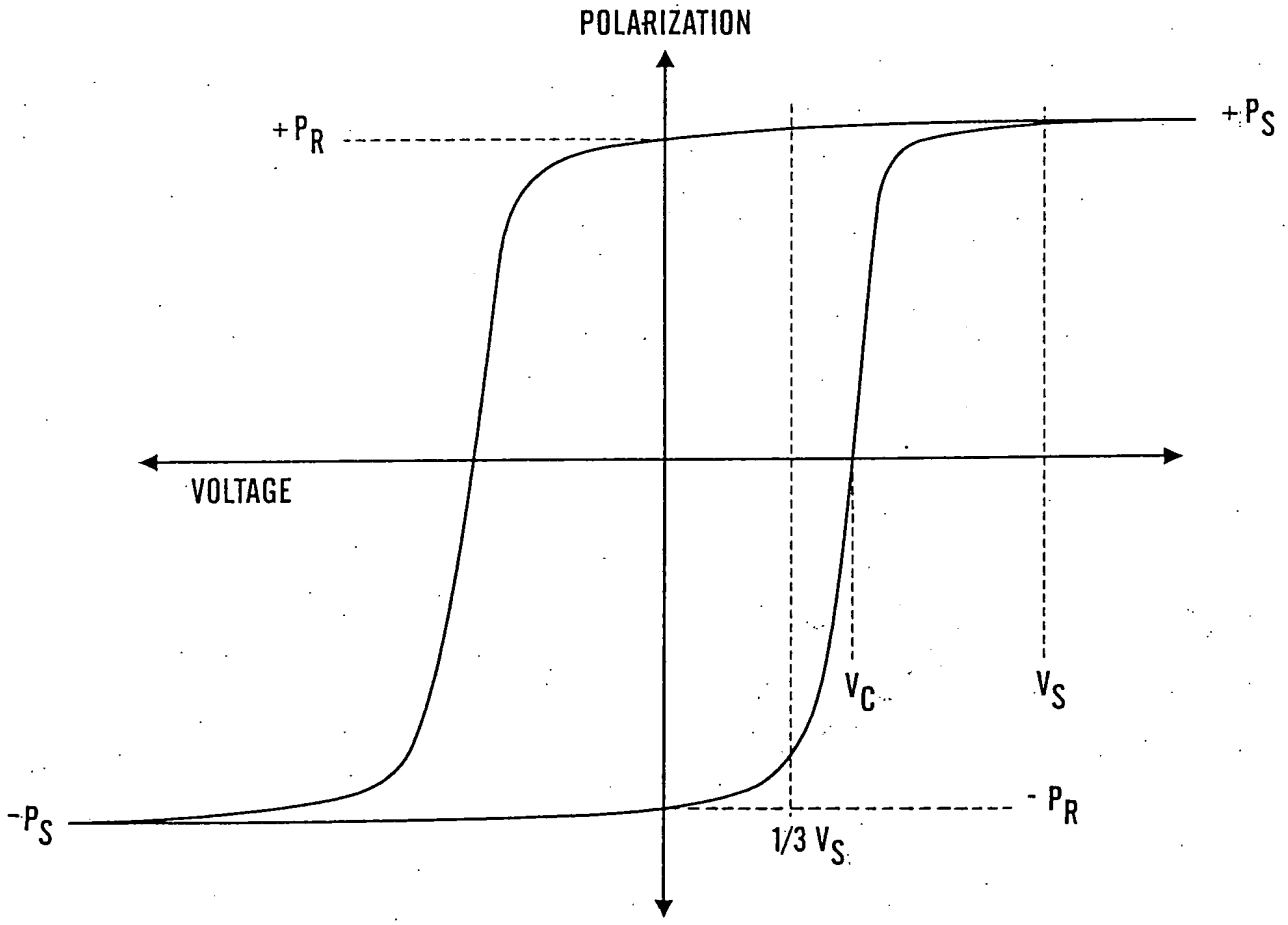

Fig. 1

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JC16

Fig.2

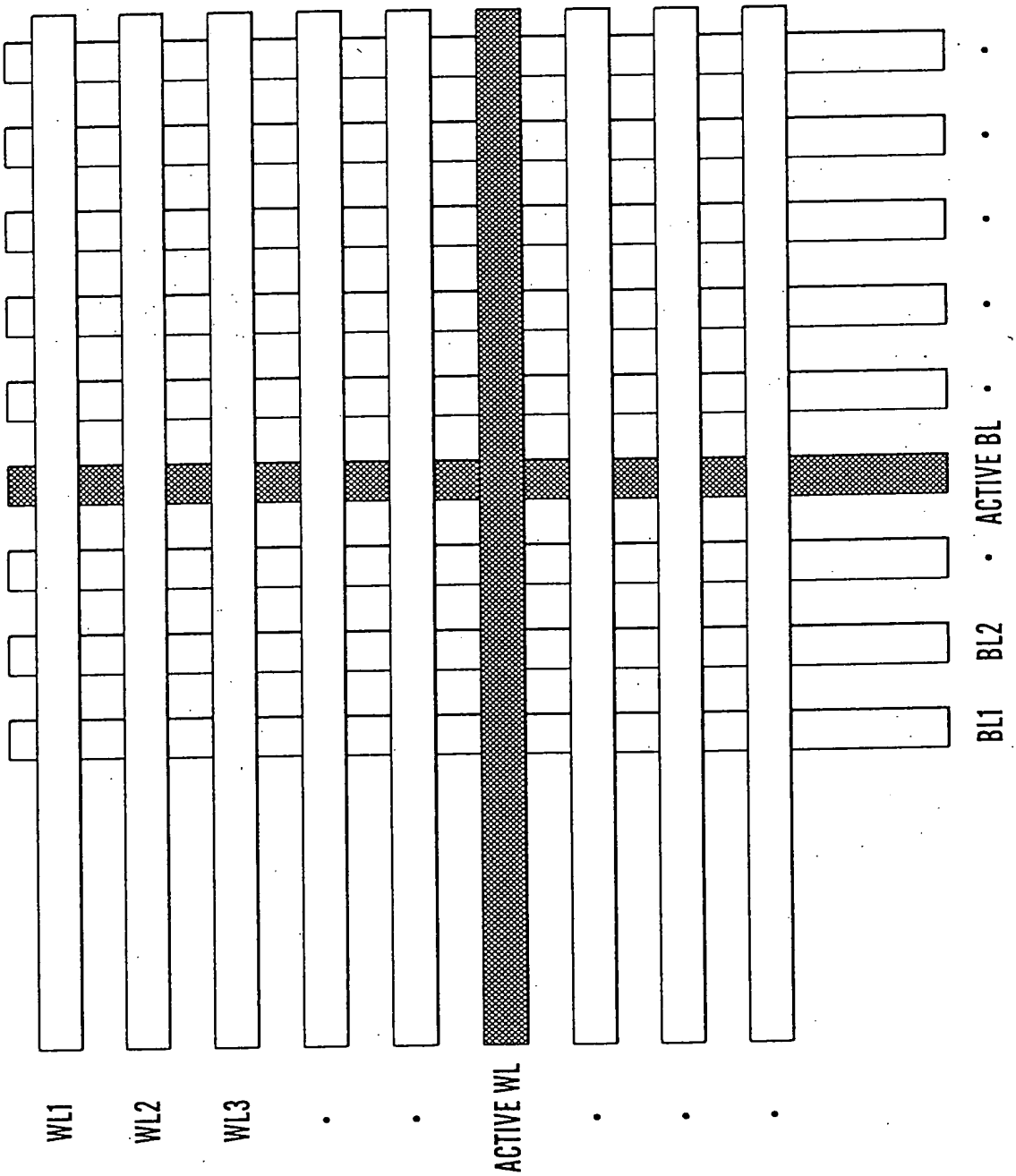

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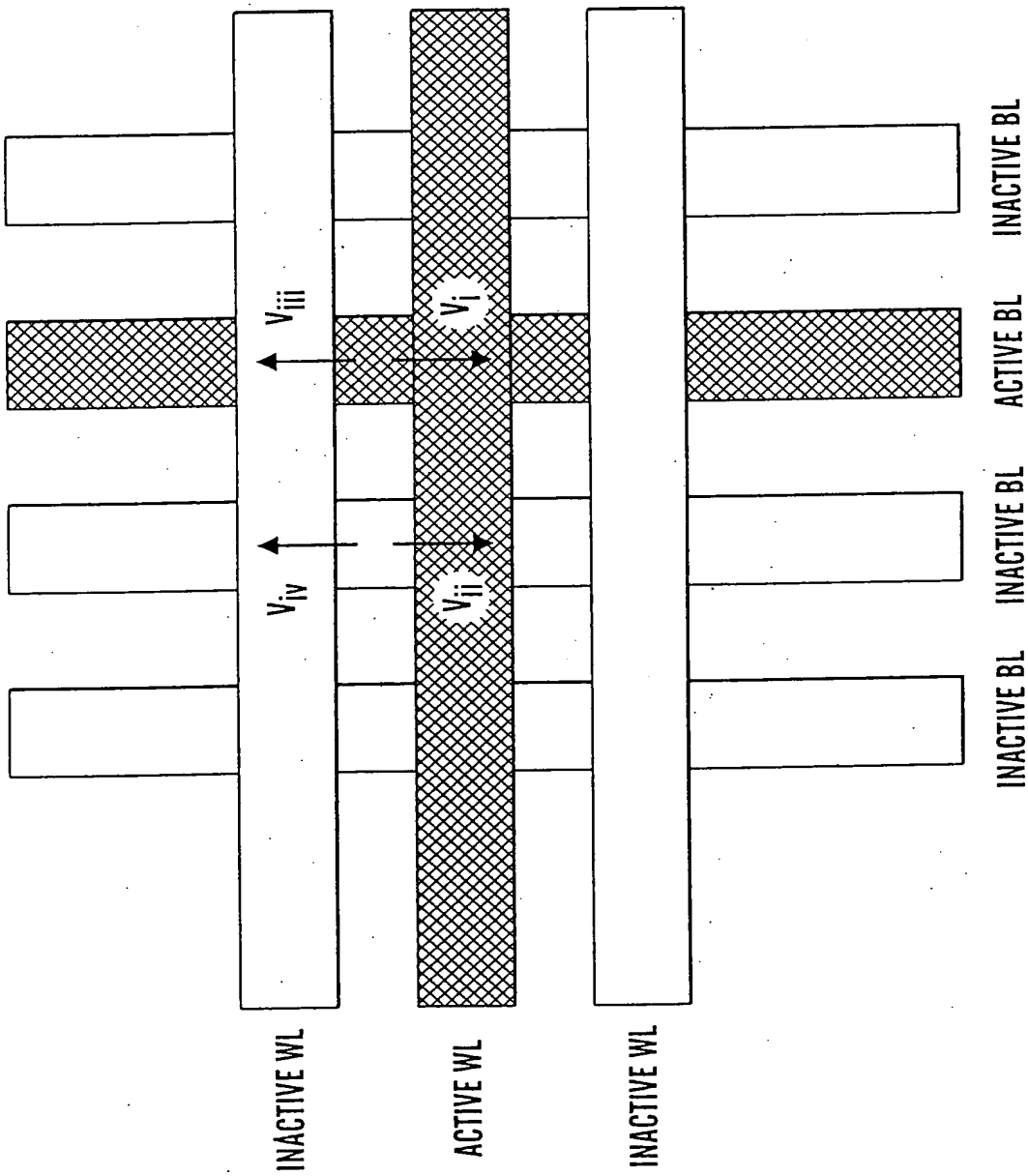
Fig.3



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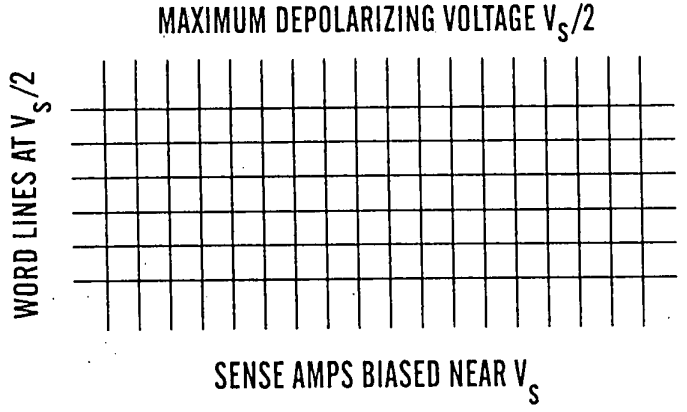
- t_0: WORD LINE LATCHED, ACTIVE PULLDOWN TO 0
- t_1: BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2: BIT LINE DECISION - DATA LATCHED
- t_3: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4: WRITE DATA LATCHED ON BIT LINES
- t_5: WORD LINE PULLED TO V_s - SET/RESET CAPS
- t_6: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7: BIT LINES ACTIVELY RETURNED TO V_s CLAMP
- t_8: READ/WRITE CYCLE COMPLETE



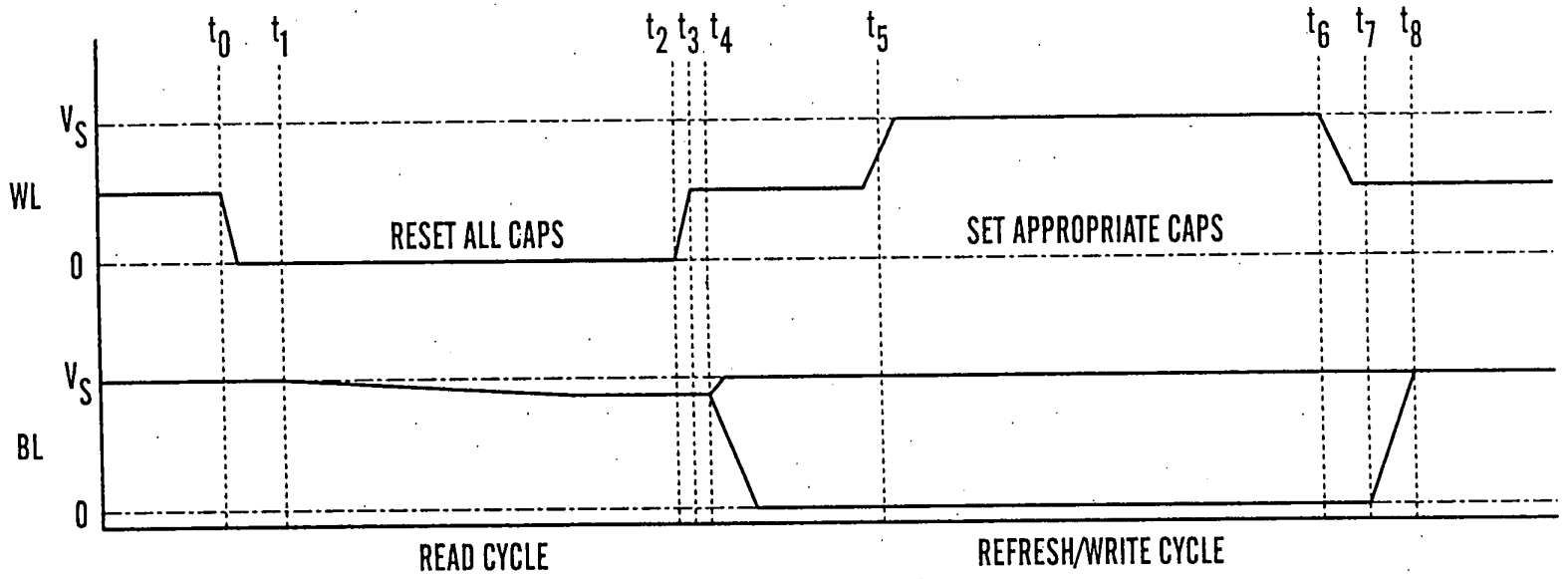


Fig.4

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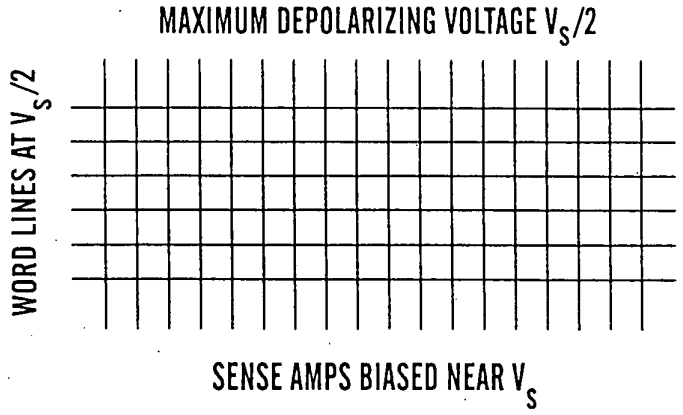
- t_0: WORD LINE LATCHED, ACTIVE PULL UP TO V_S
- t_1: BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2: BIT LINE DECISION - DATA LATCHED
- t_3: WORD LINE RETURNED TO QUIESCENT $V_S/2$
- t_4: WRITE DATA LATCHED ON BIT LINES
- t_5: WORD LINE PULLED TO 0 - SET/RESET CAPS
- t_6: WORD LINE RETURNED TO QUIESCENT $V_S/2$
- t_7: BIT LINES ACTIVELY RETURNED TO 0 CLAMP
- t_8: READ/WRITE CYCLE COMPLETE



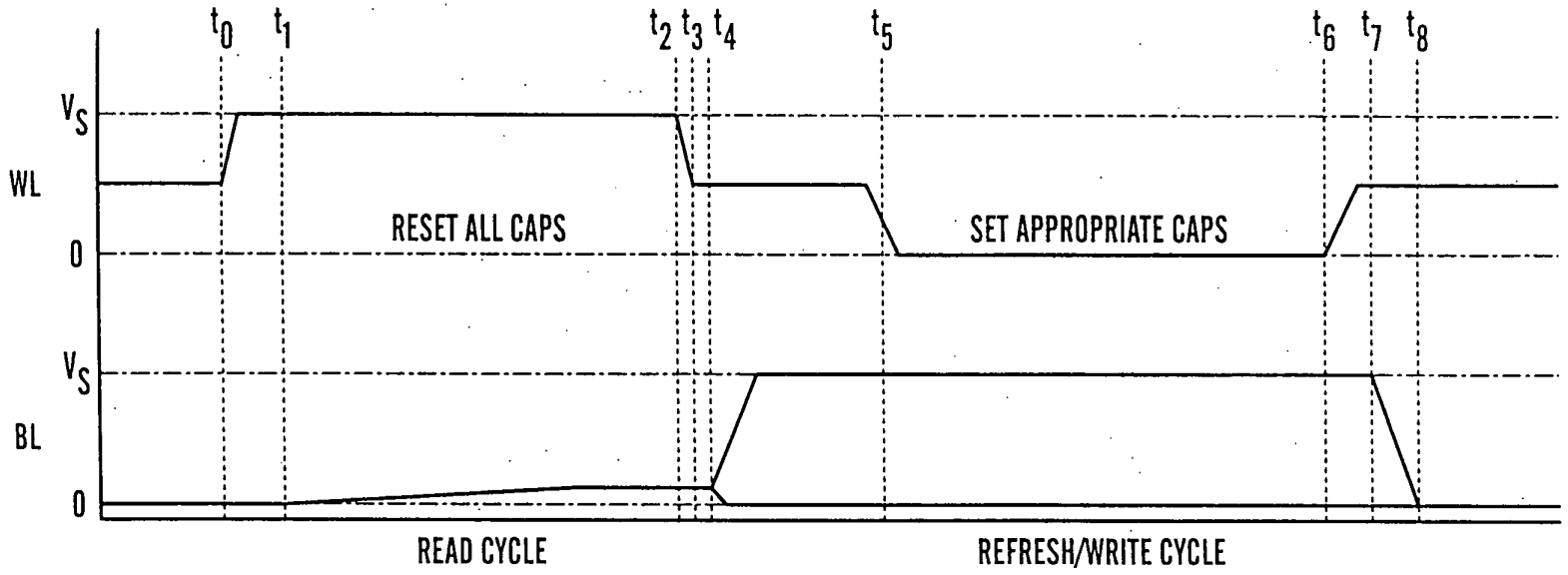


Fig.5

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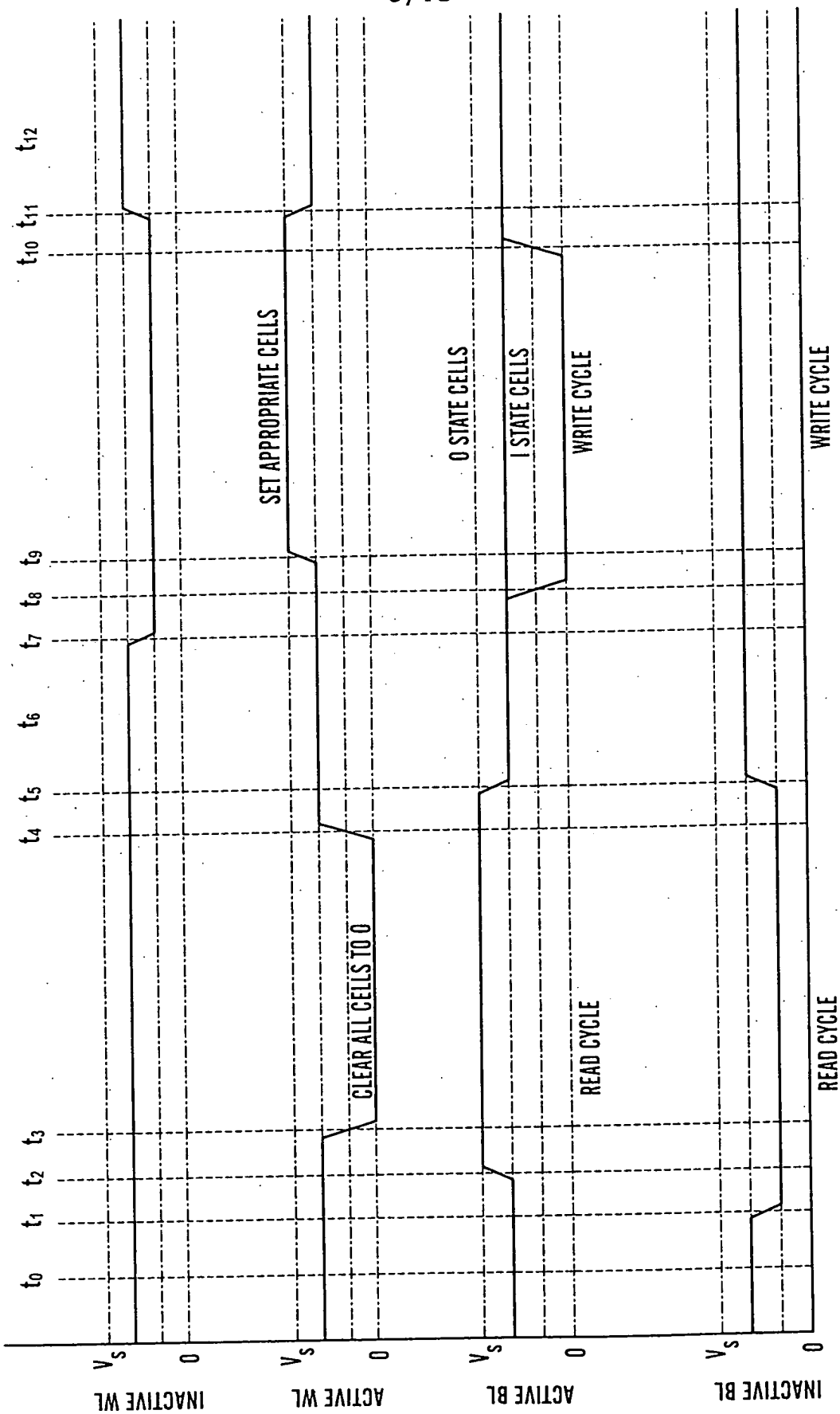

Fig.6

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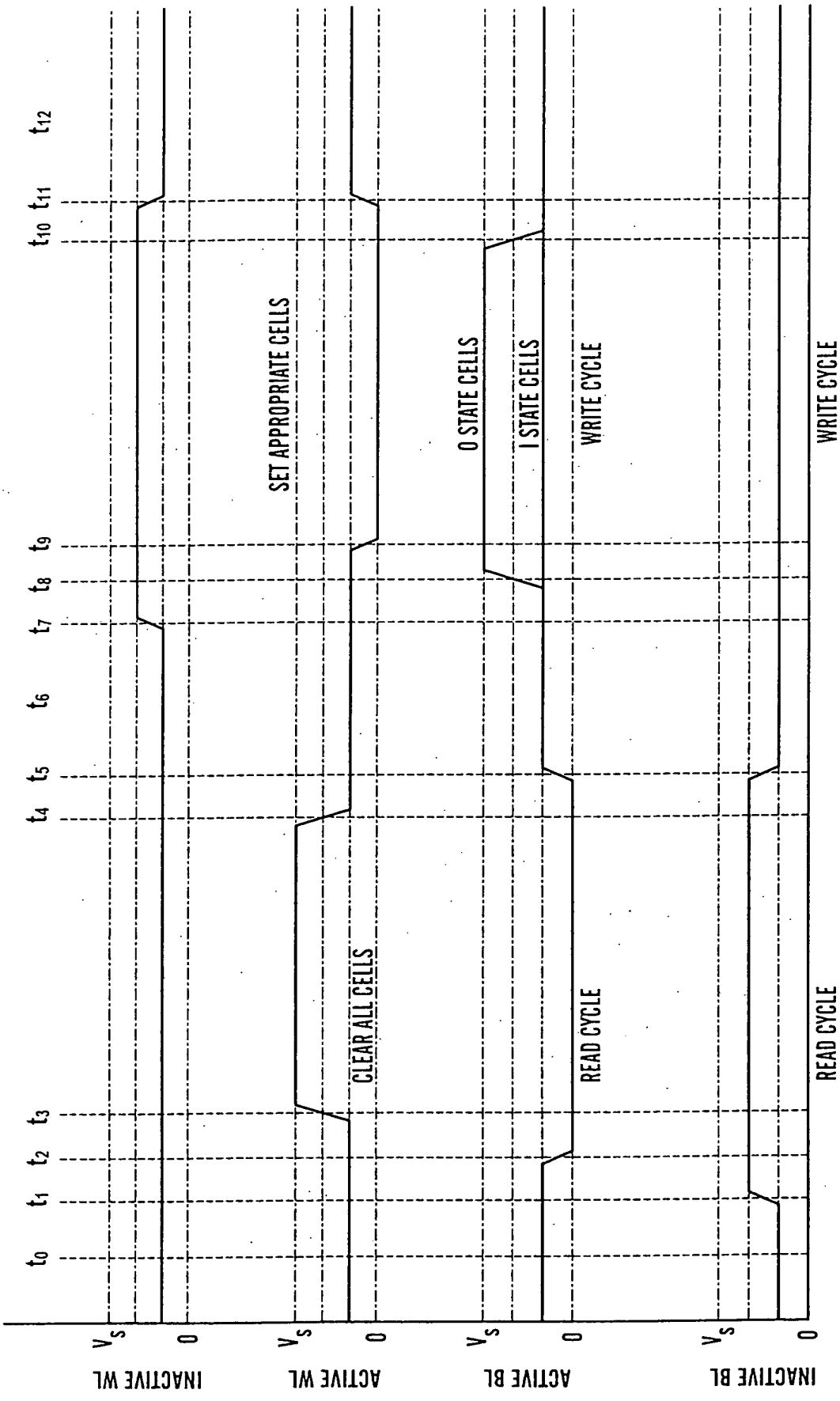

Fig.7

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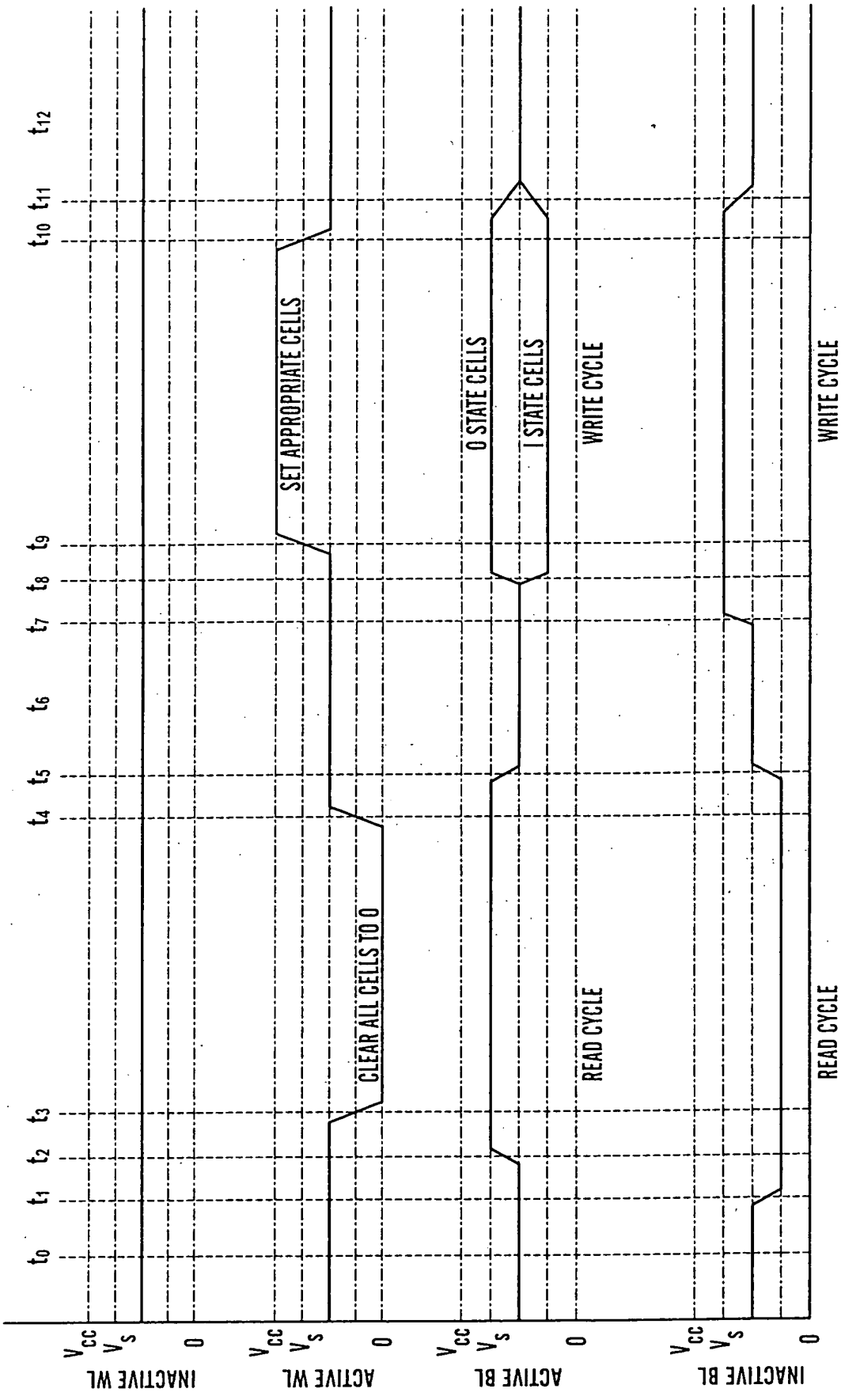

Fig.8

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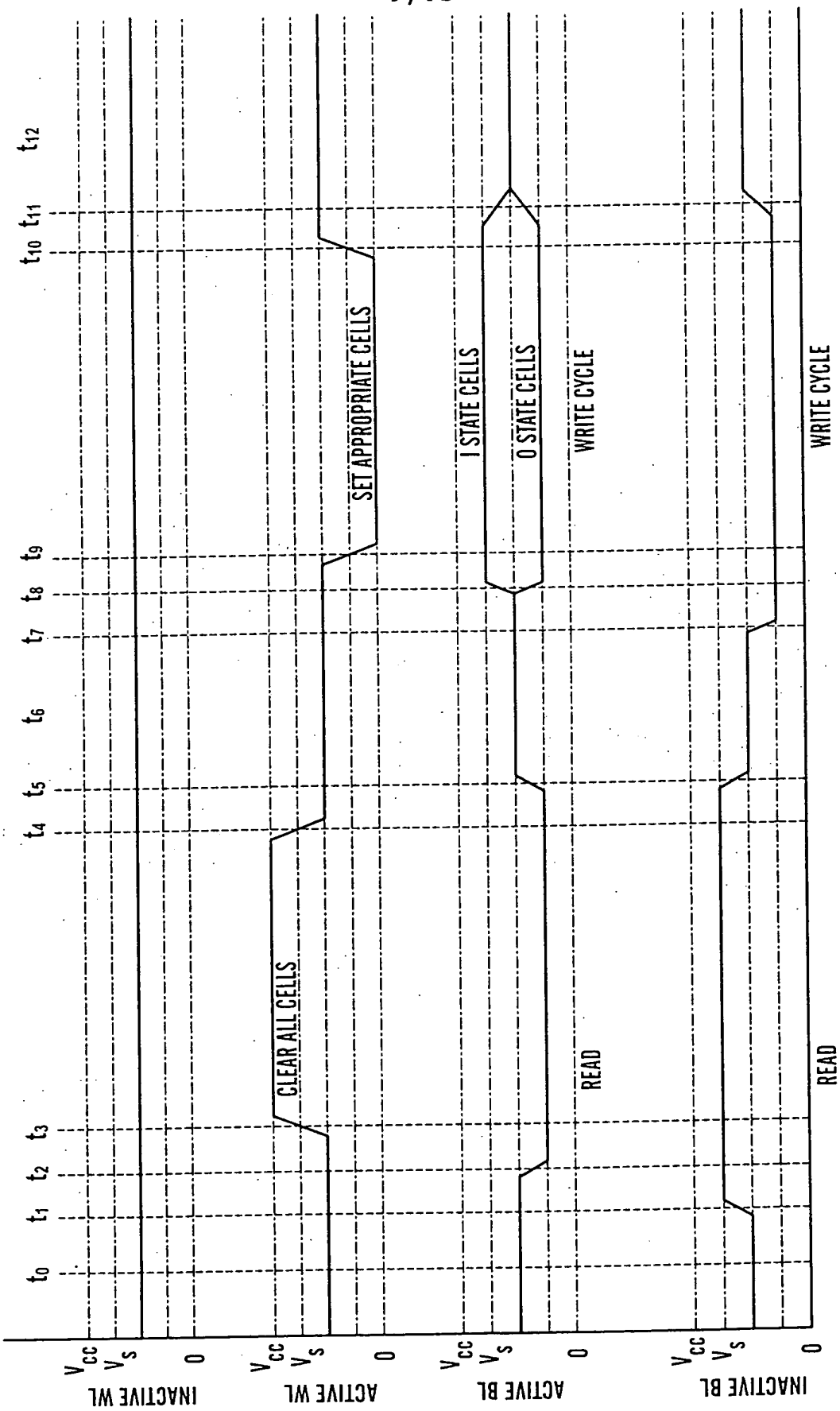

Fig.9

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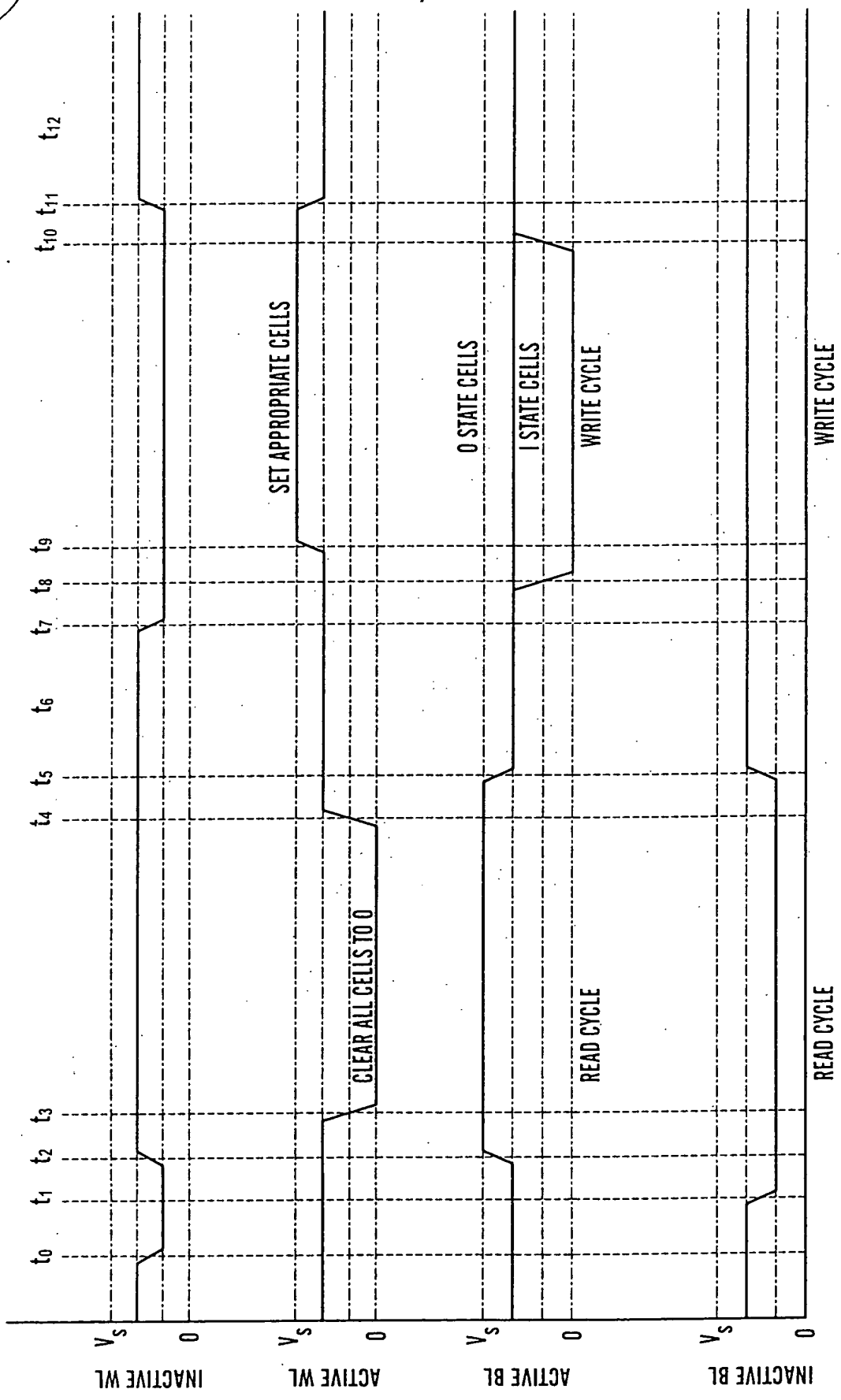

Fig. 10

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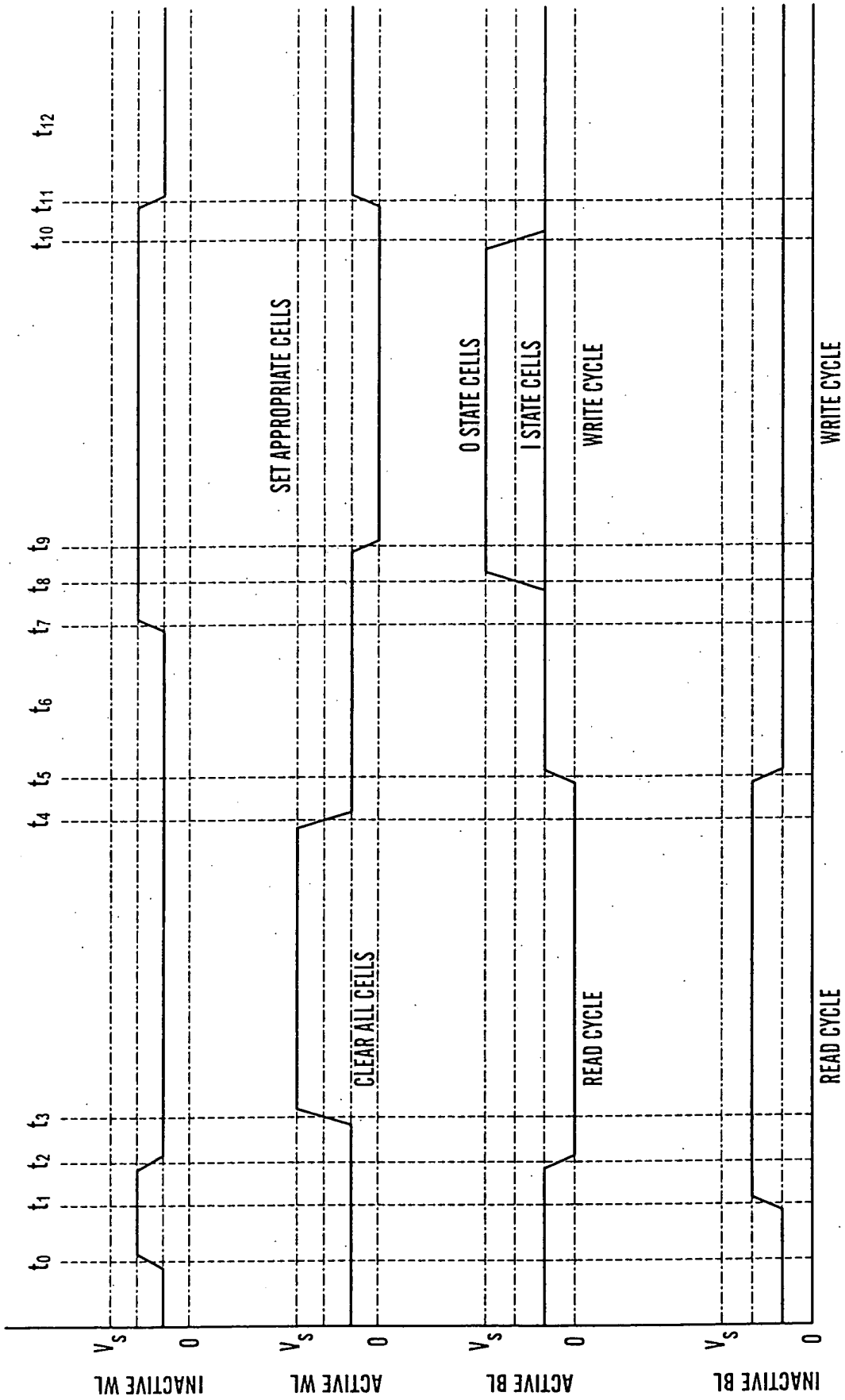

Fig. 11

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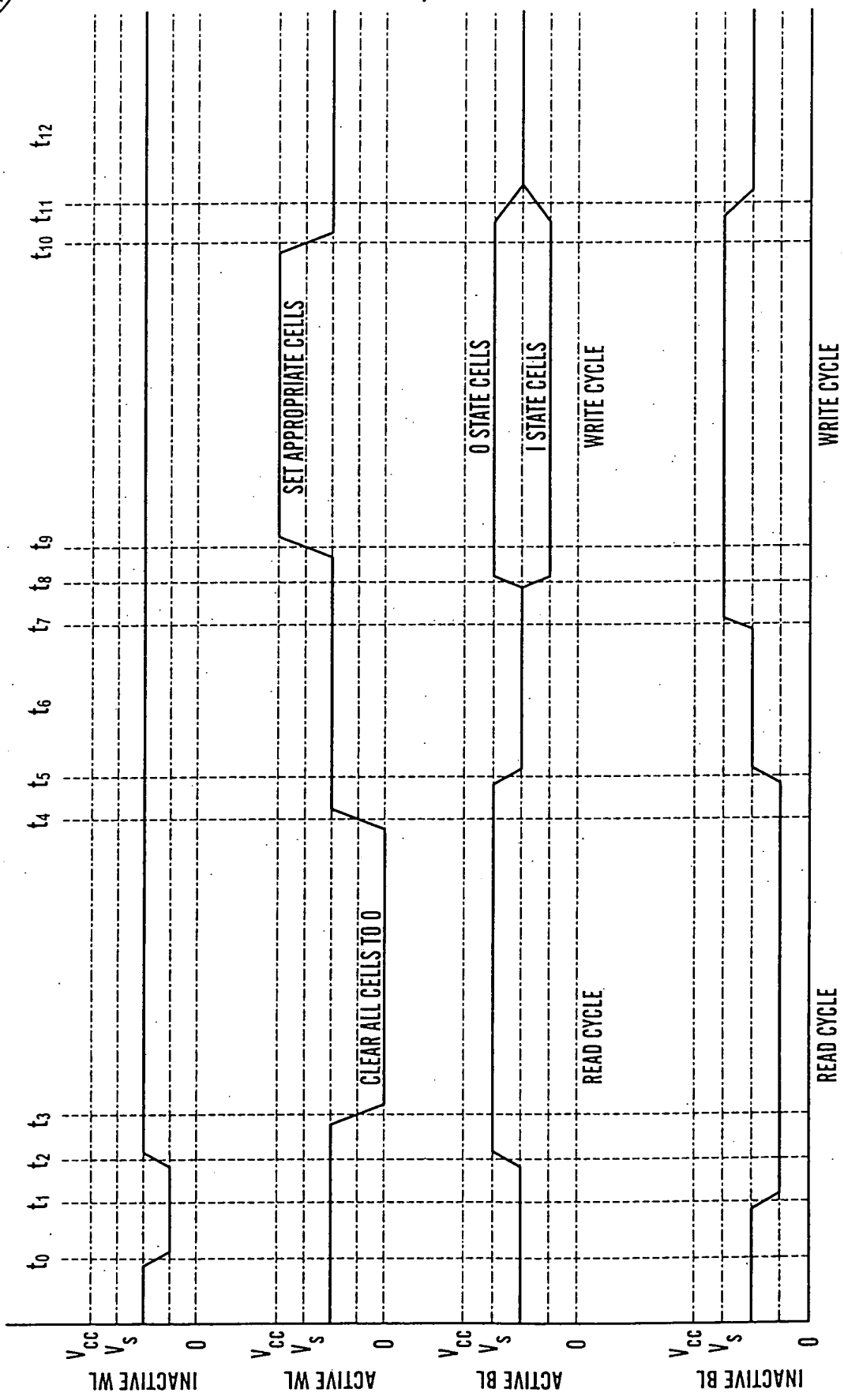

Fig. 12

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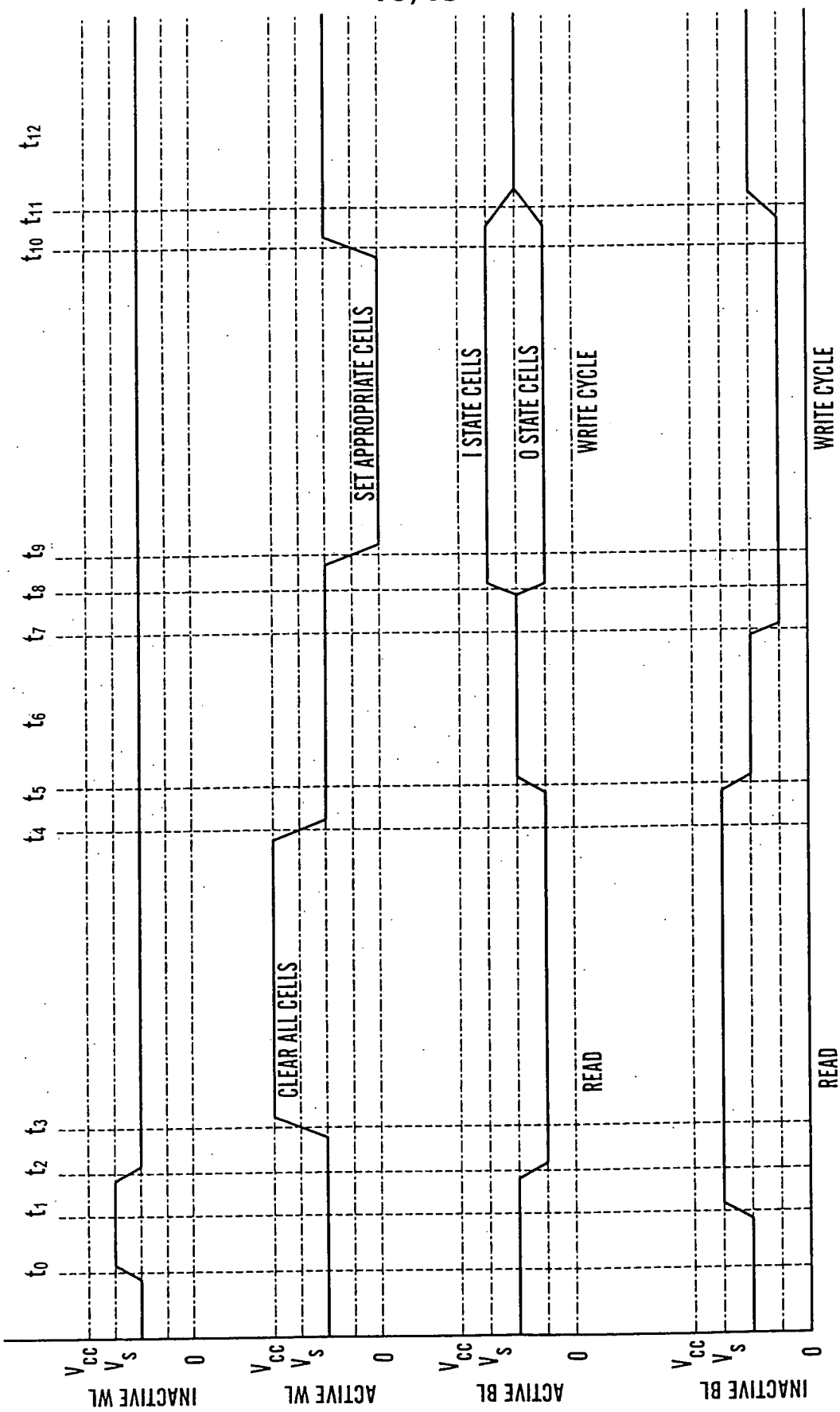

Fig. 13

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EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE

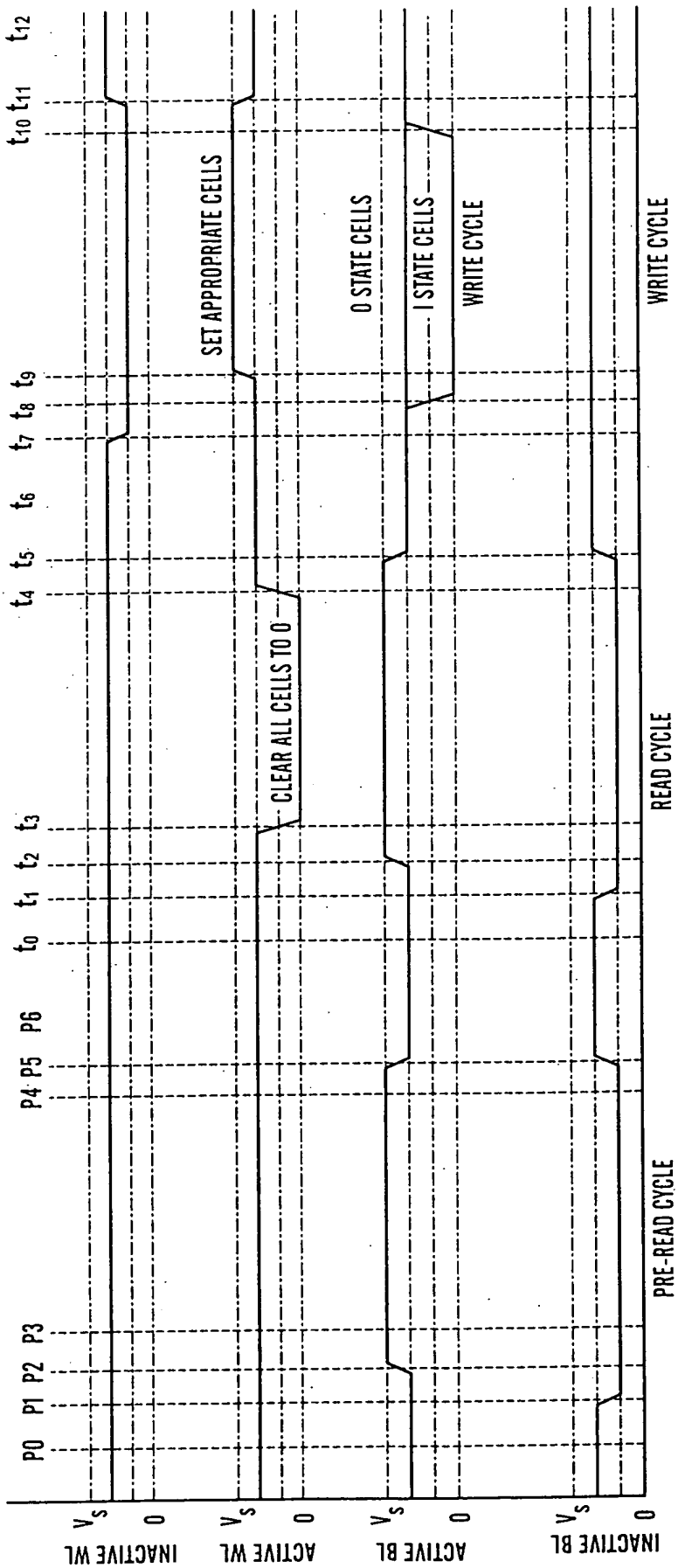

Fig. 14

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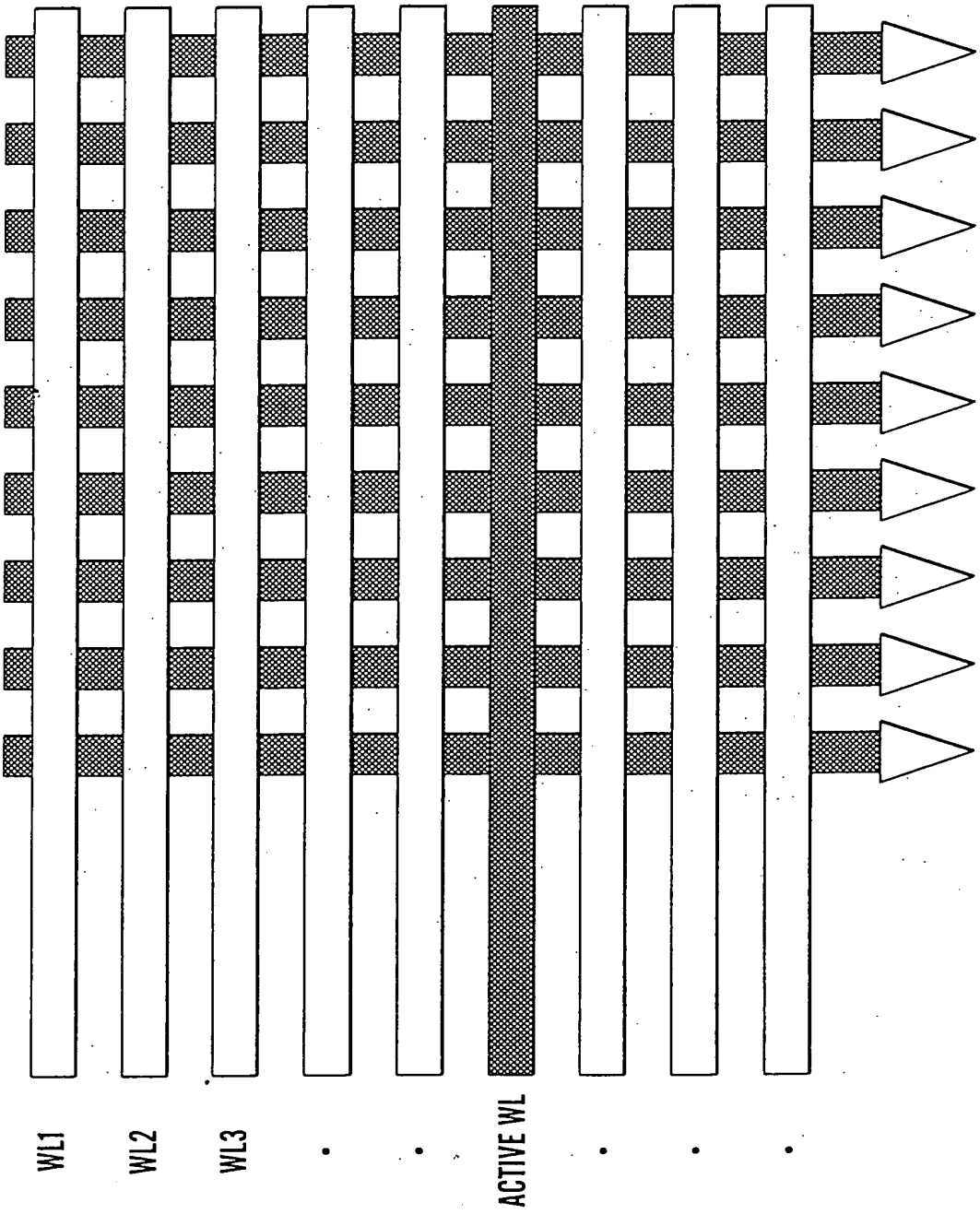

Fig.15